REMARKS

In the present application, claims 1-12 stand rejected and remain pending. Reconsideration of the application is respectfully requested.

First Rejection Under 35 U.S.C. § 103

The Examiner rejected claims 1, 2, 5 and 6 under 35 U.S.C. § 103(a) as being unpatentable over Harte (U.S. Pat. No. 5,794,137). The rejection is too lengthy to be reproduced efficiently herein. Nonetheless, Applicants respectfully traverse this rejection.

The burden of establishing a *prima facie* case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214 U.S.P.Q. 735 (PTO Bd. App. 1979). Obviousness cannot be established by combining or modifying the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination or modification. *See ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). Accordingly, to establish a *prima facie* case, the Examiner must not only show that the combination or modification includes *all* of the claimed elements, but also a convincing line of reason as to why one of ordinary skill in the art would have found the claimed invention to have been obvious in light of the teachings of the references. *See Ex parte Clapp*, 227 U.S.P.Q. 972 (B.P.A.I. 1985). When prior art references require a selected combination or modification to render obvious a subsequent invention, there must be some reason for the combination or modification other than the hindsight gained from the invention itself, i.e., something in the prior art as a whole must suggest the desirability, and thus the obviousness, of making the combination

or modification. *See Uniroyal Inc. v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 5 U.S.P.Q.2d 1434 (Fed. Cir. 1988).

In handheld systems implementing memory devices, for example, a standby or sleep state is typically implemented to maintain power to certain components of the devices when the system is not in use. Disadvantageously, devices may still exhibit some leakage current, even while they are in the standby or sleep state. *See* Application, page 3, lines 15-22. Leakage current is typically produced from complimentary metal oxide semiconductor (CMOS) technology that is used to manufacture SRAM and DRAM devices. *See* Application, page 4, lines 1-4. To address this concern and others, the present application discloses a device, such as a memory device, comprising an internal power supply bus and an isolation circuit. By providing an isolation circuit configured to disconnect an external power signal from an internal power supply bus in the device, the leakage mechanisms can be further reduced or eliminated when the device is in standby mode. *See* Application, page 8, lines 20 – 21.

For instance, in one exemplary embodiment, the isolation circuit may be used to disconnect a CMOS inverter on an SRAM/DRAM chip from the power signal Vcc, which may be delivered by an external power supply. *See* Application, page 7, lines 1-7. The junction leakage current is reduced or eliminated because the isolation circuit disconnects the internal power supply bus (which carries an internal voltage signal Vccx to various elements within the SRAM/DRAM chip) from the external voltage source. *See* Application, page 8, line 20 – page 9, line 12. Thus, the isolation circuit may be configured to reduce the leakage current and to provide a true "zero-power" standby mode.

Accordingly, independent claim 1 recites, a processor, a power supply coupled to the processor, and a device coupled to the processor and the power supply. The device comprises "an internal power supply bus configured to receive a power signal from the power supply, and an isolation circuit configured to disconnect the internal power supply bus from the power supply by interrupting the flow of the power signal."

In contrast to the claimed subject matter, the Harte reference does not disclose a device comprising an *internal* power supply bus and an isolation circuit, as recited in the present claims. In his rejection of the claim 1, the Examiner cited the power control 250 as correlating to the "device," and cited the fifth power bus 255 and sixth power bus 265 as correlating to the "internal power supply bus." However, in the Harte reference, the fifth power bus 255 and the sixth power bus 265 are not *internal* to the power control 250. The fifth power bus 255 connects the power control circuit 250 with the DSP 210, while the sixth power bus 265 connects the control circuit 250 with the display 225. Harte, Fig. 2; col. 4, lines 45-51. Clearly, each of the power buses 255 and 265 are external to the power control circuit 250. Accordingly, even if the power control circuit 250 could be correlated with the device recited in claim 1, it is clear that the power buses 255 and 265 can hardly be characterized is internal power supply buses of the power control circuit 250. Accordingly, the Harte reference *does not* disclose a device comprising "an internal power supply bus configured to receive a power signal from the power supply," as recited in claim 1.

Furthermore, the Harte reference does not disclose or suggest a device comprising "an isolation circuit configured to disconnect the internal power supply bus from the power supply," as

recited in claim 1. As previously discussed, the Examiner cited the power control circuit 250 as correlating with the presently recited device. However, the reference is devoid of any discussion of anything in the power control circuit 250 that disconnects an internal power supply bus within the power control circuit 250 from the battery 245. Accordingly, the reference does not disclose or suggest a device comprising anything that could be construed as an isolation circuit, much less a device comprising "an isolation circuit configured to disconnect the internal power supply bus from the power supply."

Because the Harte reference does not disclose or suggest all of the features recited in claim 1, it cannot possibly render the claimed subject matter obvious. Further, claims 2, 5 and 6 are also allowable based on the subject matter that they independently recite, as well as their dependency on allowable claim 1. Accordingly, Applicants respectfully request withdrawal of the Examiner's rejection and allowance of claims 1, 2, 5 and 6.

Second Rejection Under 35 U.S.C. § 103

The Examiner rejected claims 3, 4 and 8-11 under 35 U.S.C. § 103(a) as being unpatentable over Harte (U.S. Pat. No. 5,794,137) in view of Larsen et al. (U.S. Pat. No. 5,338,978). Applicants respectfully traverse this rejection.

Claims 3, 4 and 8-11 are patentable because the Larsen et al. reference does not cure the deficiencies of the Harte reference. In the rejection, the Examiner admitted that the Harte reference does not disclose the system comprising "a personalized digital assistant (PDA)," as recited in claim 3 or "a handheld computer," as recited in claim 4. Further, the Examiner admitted that the Harte reference does not disclose the system comprising: "an input buffer

comprising a control line configured to control the isolation circuit," as recited in claim 8; a system, "wherein the isolation circuit comprises a p-channel field effect transistor (FET), as recited in claim 9; "the gate of the p-channel FET being coupled to the control line of the input buffer," as recited in claim 10; or "an output buffer configured to buffer the device from the remainder of the system," as recited in claim 11. To disclose the recited features, the Examiner relied on the Larsen et al. reference. Whether the Larsen reference discloses such features is immaterial, because the Larsen et al. reference does not obviate the deficiencies of the Harte reference discussed with reference to independent claim 1. As a result, the cited references, either alone or in combination, do not teach, suggest, or disclose all of the recited features of the claims. Therefore, claims 3, 4 and 8-11 are patentable by virtue of their dependency from independent claim 1, as well as by virtue of their own recited subject matter. Accordingly, Applicants respectfully request withdrawal of the Examiner's rejection and allowance of claims 3, 4 and 8-11.

Third Rejection Under 35 U.S.C. § 103

The Examiner rejected claim 7 under 35 U.S.C. § 103(a) as being unpatentable over Harte (U.S. Pat. No. 5,794,137) in view of Keeth et al. (U.S. Pat. No. 6,400,595). Applicants respectfully traverse this rejection. However, the rejection is moot, as Applicants have chosen to remove the reference as prior art.

In accordance with 35 U.S.C.§ 103(c) and Pub. L. 106-113, § 4807, enacted November 29, 1999, subject matter developed by another person which qualifies as prior art only under subsection (e) of 35 U.S.C.§ 102, shall not preclude patentability where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or

subject to an obligation of assignment to the same person. Here, both the subject matter of the Keeth et al. reference and the claimed invention were, at the time the invention was made, owned by the present assignee (Micron) or subject to an obligation of assignment to the present assignee. Since the present application has a filing date after November 29, 1999, the Keeth et al. reference does not qualify as prior art under 35 U.S.C.§ 102(e)/103(c).

In the rejection, the Examiner admitted that the Harte reference fails to disclose "the isolation circuit is coupled between a pad on the device configured to receive the power signal and the internal power supply bus, as recited in claim 7. Regardless of whether the Keeth et al. reference discloses these features, without the Keeth et al. reference, the Examiner's rejection cannot stand. Claim 7 depends from independent claim 1, and is believed to be allowable for the subject matter independently recited in the claim, as well as the subject matter recited in the allowable base claim. Because the Harte reference does not disclose or suggest the subject matter as set forth in the rejected claim, as discussed above, the reference cannot render it obvious. Therefore, Applicants respectfully request withdrawal of the Examiner's rejection and allowance of claim 7.

Fourth Rejection Under 35 U.S.C. § 103

The Examiner rejected claims 8-11 under 35 U.S.C. § 103(a) as being unpatentable over Harte (U.S. Pat. No. 5,794,137) in view of Klughart et al. (U.S. Pat. No. 6,396,137 B1). Applicants respectfully traverse this rejection.

Claims 8-11 depend from independent claim 1, and are believed to be patentable for the subject matter recited in each of the dependent claims. In addition, claims 8-11 are patentable because the Klughart et al. reference does not cure the deficiencies of the Harte reference. As a result, the cited references, either alone or in combination, do not teach, suggest, or disclose all of the recited features of the claims. Therefore, claims 8-11 are patentable by virtue of their dependency from independent claim 1, as well as by virtue or their own recited subject matter. Accordingly, Applicants respectfully request withdrawal of the Examiner's rejection and allowance of claims 8-11.

Fifth Rejection Under 35 U.S.C. § 103

The Examiner rejected claim 12 under 35 U.S.C. § 103(a) as being unpatentable over Harte (U.S. Pat. No. 5,794,137) in view of Klughart et al. (U.S. Pat. No. 6,396,137 B1) and Keeth et al. (U.S. Pat. No. 6,400,595). Applicants respectfully traverse this rejection.

As discussed above, both the subject matter of the Keeth et al. reference and the claimed invention were, at the time the invention was made, owned by the present assignee (Micron) or subject to an obligation of assignment to the present assignee. Accordingly, the Keeth et al. reference does not qualify as prior art under 35 U.S.C.§ 102(e)/103(c). In the rejection, the Examiner relied on the Keeth et al. reference to provide a circuitry coupled between the output buffer and the input/output pad and configured to tri-state the input/output pad, which was not disclosed or suggested by Klughart or Harte. Regardless of whether the Keeth et al. reference discloses these features, without the Keeth et al. reference, the Examiner's rejection cannot stand. Accordingly, Applicants respectfully request withdrawal of the Examiner's rejection and allowance of claim 12.

Conclusion

In view of the remarks set forth above, Applicants respectfully request withdrawal of the Examiner's rejections and allowance of claims 1-12. If the Examiner believes that a telephonic interview will help speed this application toward issuance, the Examiner is invited to contact the undersigned at the telephone number listed below.

General Authorization for Extensions of Time

In accordance with 37 C.F.R. § 1.136, Applicants hereby provide a general authorization to treat this and any future reply requiring an extension of time as incorporating a request therefore. Furthermore, Applicants authorize the Commissioner to charge the appropriate fee for any extension of time to Deposit Account No. 13-3092; Order No. MICS:0071/FLE (00-0901).

Respectfully submitted,

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